

A New RF Model for the Accumulation-Mode MOS Varactor

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Abstract — This paper presents a new RF model of an accumulation-mode MOS varactor, which is composed of the physically meaningful parameters. This model can describe the characteristics of the device with simple equations valid in all operating regions. For easy integration into common circuit simulators, a single topology with the lumped elements derived from the device structure has been proposed. With directly extracted parameters based on the Z-parameter analysis on the equivalent circuit, excellent agreements between measured data and simulation results were obtained without any optimization steps in the frequency range up to 18 GHz, as well as the overall bias range.

I. INTRODUCTION

On-chip voltage-controlled capacitors (varactors) play one of the most important roles as integrated RF passive devices. Recently, the accumulation-mode MOS varactor has been introduced as tuning element for RF applications [1]-[2] and proven to be superior to the reverse biased p-n junction varactor in terms of power consumption, phase noise, and tuning range for the integrated *LC*-tank voltage-controlled oscillators (VCOs) [3].

Several RF models for the MOS varactor have been reported in [2], [4]-[6]. The physical model proposed in [2] was derived by considering the device structure but consisted of separate models for the different operating regions of the device in accumulation and in depletion. The theoretical model reported in [4] includes the physics-based equations that complicate implementation in the SPICE-like circuit simulators. The SPICE compatible models exploiting a sub-circuit based on the BSIM3v3 model were presented in [5]-[6]. However, there were large deviations in the measured and simulated quality factor-voltage (*Q*-V) characteristics due to the constant series resistance. To accurately describe the *Q*-V behaviors of the device over whole bias range, the bias dependence of the series resistance should be included in the model with new equation.

In this paper, we proposed a novel equivalent circuit valid in all regions of operation with the simple semi-empirical equations for RF MOS varactor. Also efficient and accurate direct parameter extraction from analysis for

the measured *Z*-parameters on this equivalent circuit was developed. As a result, highly accurate prediction for *C*-*V* and *Q*-*V* characteristics was obtained.

II. NEW EQUIVALENT CIRCUIT

The cross-section of an accumulation-mode MOS varactor fabricated in a standard CMOS process is shown in Fig. 1. The new equivalent circuit derived from Fig. 1 is shown in Fig. 2. In Fig. 2, C_s refers to the series connection of the gate oxide capacitance and the depletion capacitance in the silicon under the gate oxide. C_f represents the fringing capacitance mainly associated with the sidewall of the gate. L_g and R_{poly} are the parasitic inductance and distributed resistance of the gate electrode, respectively. For accurate modeling of the gate bias dependence of the channel resistance (R_{ch}), R_{acc} , R_p , and R_s are used. R_{acc} represents the resistance of the accumulation layer formed in the channel region. R_p is the n-well resistance in parallel with R_{acc} and R_s is the gate bias independent resistance of R_{ch} in series with the parallel connection of R_{acc} and R_p . The resistance in the source/drain regions is represented by R_{sd} . R_{well} is the vertical resistance of n-well, C_{sub1} is the depletion capacitance between n-well and p-substrate, and the parallel combination of R_{sub} and C_{sub2} models the lossy silicon substrate.

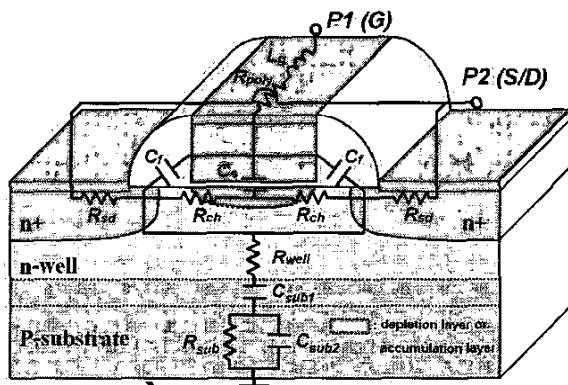


Fig. 1. Cross-section of an accumulation-mode MOS varactor.

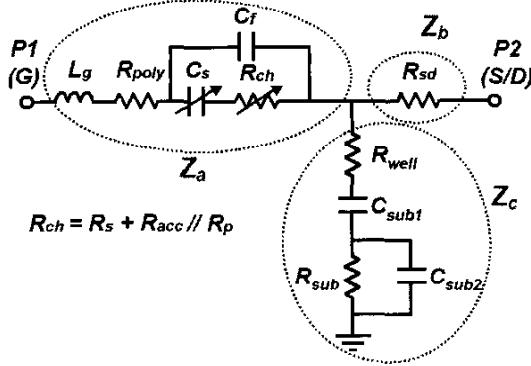


Fig. 2. New equivalent circuit of an accumulation-mode MOS varactor.

III. DIRECT EXTRACTION AND MODEL VERIFICATION

To verify the proposed equivalent circuit as shown in Fig. 2, we have characterized the accumulation-mode MOS varactors fabricated in a standard 0.18- μm CMOS process with the bulk substrate resistivity of about 1 $\Omega\cdot\text{cm}$. The fabricated MOS varactors have an identical unit finger width (W) of 2 μm and an identical number of fingers (F) of 50, except having the different gate lengths (L 's) of 0.50 μm , 0.35 μm , and 0.18 μm . Direct parameter extraction was performed with Z-parameter analysis on the equivalent circuit without any optimization steps. If optimization is involved, there is a possibility of obtaining non-physical values of parameters [7]-[8]. Two-port S -parameters were measured in a frequency range from 0.5 GHz to 18 GHz for devices using an HP8510C network analyzer and a Summit 11742 probe station and the two-step de-embedding was carried out.

In order to clearly illustrate the direct parameter extraction procedure, we have characterized the test device with L of $0.50 \mu\text{m}$. Assuming that $aR_{ch}CsC_f \ll C_s + C_f$ and $a^2R_{ch}^2C_s^2C_f \ll C_s + C_f$ from the analysis of Z-parameters on the equivalent circuit shown in Fig. 2, we can define $R_{g,eff}$ and $C_{g,eff}$ as the following equations,

$$R_{g,eff} \approx R_{poly} + R_{ch} \left(C_s / C_{g,eff} \right)^2, C_{g,eff} \approx C_s + C_f \quad (1)$$

With (1), the Z-parameters are given by,

$$Z_a = Z_{11} - Z_{12} = R_{a,eff} + j(\omega L_a - 1/\omega C_{a,eff}) \quad (2)$$

$$Z_1 \equiv Z_\infty = Z_{\infty 1} \equiv R_1 \quad (3)$$

$$Z_c = Z_{12} = R_{well} + \frac{R_{sub}}{1 + \omega^2 R_{sub}^2 C_{sub2}^2} - j \left(\frac{1}{\omega C_{sub1}} + \frac{\omega R_{sub}^2 C_{sub2}}{1 + \omega^2 R_{sub}^2 C_{sub2}^2} \right) \quad (4)$$

Using (2), $R_{g,eff}$ was extracted by averaging $\text{Re}(Z_a)$ with varying frequency and $C_{g,eff}$ was extracted from $-1/\omega\text{Im}(Z_a)$ in the frequency range below 5 GHz, where the influence of L_g is negligible in $\text{Im}(Z_a)$. L_g was analytically determined from $\text{Im}(Z_a)$ in (2). The gate bias dependences of $R_{g,eff}$ and $C_{g,eff}$ are shown in Fig. 3. The tuning range (C_{max} / C_{min}) was about 3.2 and the effective resistance was about 2.7Ω at $V_g = 0$ V. C_f was obtained by extrapolating the $C_{g,eff}$'s of the three test devices with different L 's of $0.50 \mu\text{m}$, $0.35 \mu\text{m}$, and $0.18 \mu\text{m}$, as shown in Fig. 4. $R_{poly} = (1/3) \times R_{poly,sh} \times (W_f/L_f) / N_f$ was calculated to be 0.19Ω [9].

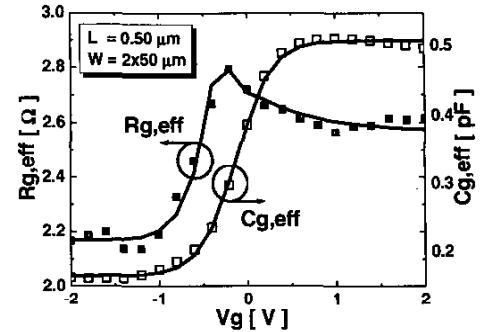


Fig. 3. Gate bias dependences of the extracted (symbol) and modeled (solid line) $R_{g,eff}$ and $C_{g,eff}$.

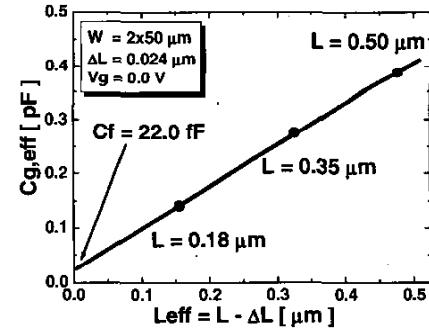


Fig. 4. Parameter extraction of C_f at $V_g = 0$ V.

Then, C_s and R_{ch} were calculated by using (1) as shown in Fig. 5. To model the gate bias dependence of C_s and R_{ch} , we used the simple equations as follows,

$$C_s = C_{s,\min} + \frac{dC_s}{2} \times \left[1 + \tanh \left(\frac{V_g - dV_{g,s}}{V_{g,norm,s}} \right) \right] \quad (5)$$

$$R_{\perp} \equiv R_{\parallel} + R_{\perp} \parallel R_{\perp} \quad (6)$$

$$R_{acc} = \begin{cases} 1/K_{acc}(V_g - dV_{g,th}), & \text{if } V_g > dV_{g,th} \\ \infty, & \text{elsewhere} \end{cases} \quad (7)$$

(5) is an empirical equation based on [9]-[10], and it can accurately describe the nonlinear characteristic of C_s with varying gate bias, as shown in Fig. 5. In (6), R_{acc} is the resistance of the accumulation layer and R_s is the bias-independent resistance in series with R_{acc} . R_p is the effective resistance between R_s and the edge of the depletion layer. (7) is a semi-empirical equation that assumes R_{acc} is inversely proportional to $V_g - dV_{g,th}$. In (7), K_{acc} is the parameter that is related to the mobility of electrons in the accumulation layer, and $dV_{g,th}$ is relevant to the flat-band voltage (V_{fb}). When V_g decreases below V_{fb} , R_{acc} can be considered as infinite and R_{ch} approaches a constant value of $R_s + R_p$. When V_g increases above V_{fb} , R_{acc} dominates in R_{ch} and hence R_{ch} decreases and finally approaches a constant value of R_s , as shown in Fig. 5. The extracted values of R_{acc} , R_p , and R_s were 0.08 Ω (at $V_g = 0$ V), 1.41 Ω , and 2.51 Ω , respectively.

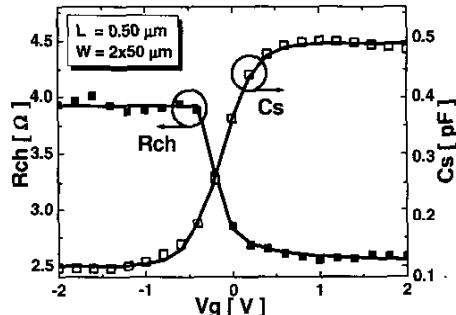


Fig. 5. Gate bias dependences of the extracted (symbol) and modeled (solid line) R_{ch} and C_s .

As shown in Fig. 6, R_{sd} was determined by averaging $Re(Z_b)$ with varying frequency using (3), and $Im(Z_b)$ remain almost zero with varying frequency. This result indicates that the proposed equivalent circuit and the corresponding parameter extraction procedure are accurate and reliable.

Finally, (4) can be rewritten as follows,

$$\frac{1}{Re[Z_c]} = \frac{1 + \omega^2 R_{sub}^2 C_{sub2}^2}{R_{well} + R_{sub} + \omega^2 R_{well} R_{sub}^2 C_{sub2}^2} \quad (8)$$

$$\frac{1}{Re[Z_c] - (R_{well} + R_{sub})} = \frac{1}{R_{sub}} + \frac{1}{\omega^2 R_{sub}^3 C_{sub2}^2} \quad (9)$$

R_{well} , R_{sub} , and C_{sub2} were extracted from the linear regression using (8) and (9) under the assumption of $R_{well} + R_{sub} \gg \omega^2 R_{well} R_{sub}^2 C_{sub2}^2$. Then, C_{sub1} was analytically determined from $Im(Z_c)$ in (4). As expected,

the substrate-related parameters, R_{well} , R_{sub} , C_{sub1} , and C_{sub2} were almost independent of gate bias as shown in Fig. 7.

The extracted parameter values are summarized in Table I. Since $\omega R_{ch} C_s C_f \approx 3.4 \times 10^{-16}$, $\omega^2 R_{ch}^2 C_s^2 C_f \approx 5.4 \times 10^{-18}$, and $C_s + C_f \approx 3.9 \times 10^{-13}$ at $V_g = 0$ V and 2.4 GHz using the extracted results, the assumption leading to (1) is validated. Fig. 8 shows the measured and simulated S -parameters at $V_g = 0$ V for the device having L of 0.50 μ m. The total error [7] between the measured and the simulated S -parameters with the proposed equivalent circuit was calculated to be only 0.045 % in the frequency range up to 18 GHz.

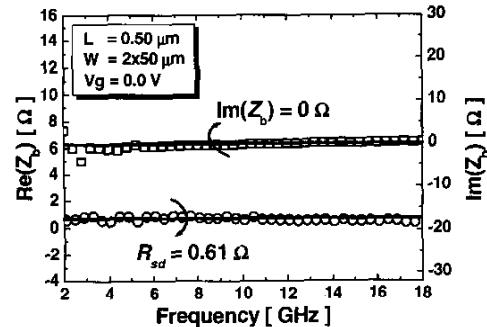


Fig. 6. Parameter extraction of R_{sd} at $V_g = 0$ V.

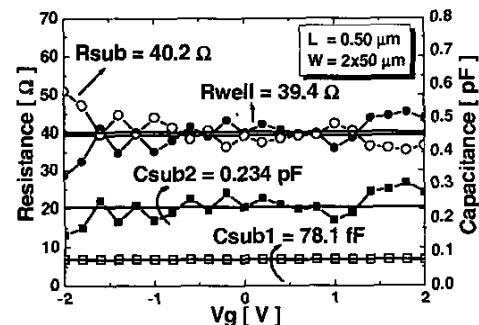


Fig. 7. Gate bias dependences of the extracted (symbol) and modeled (solid line) R_{well} , R_{sub} , C_{sub1} , and C_{sub2} .

TABLE I

EXTRACTED PARAMETER VALUES FOR THE DEVICE WITH GATE LENGTH OF 0.50- μ M AT GATE BIAS OF 0 V

Parameter s	Values	Parameters	Values
L_g	24.70 pH	R_{sd}	0.64 Ω
R_{poly}	0.19 Ω	R_{well}	40.01 Ω
R_{ch}	2.85 Ω	R_{sub}	39.23 Ω
C_s	364.62 fF	C_{sub1}	78.03 fF

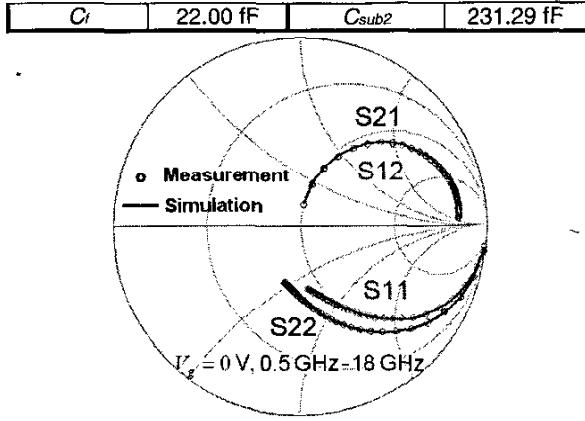


Fig. 8. Measured (symbol) and simulated (solid line) S -parameters at $V_g = 0$ V. The simulated results with the proposed equivalent circuit matched very well with measured data.

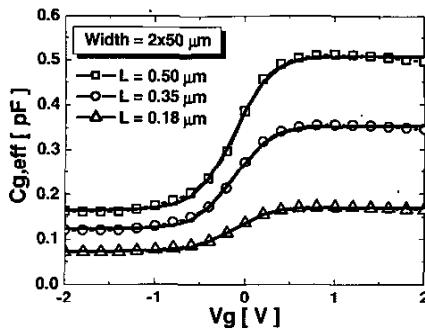


Fig. 9. Comparison of the measured (symbol) and simulated (solid-line) C - V characteristics for three test devices.

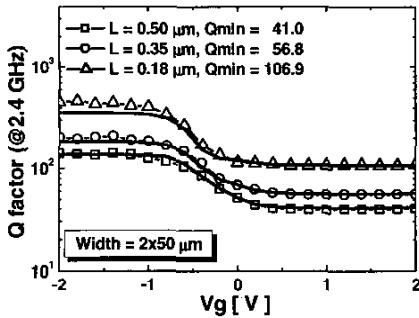


Fig. 10. Comparison of the measured (symbol) and simulated (solid-line) Q - V characteristics at 2.4 GHz for three test devices.

To further demonstrate the capability of the new equivalent circuit, direct parameter extraction was additionally performed with other test devices with different L 's as mentioned above. As a result, C - V characteristics and Q - V characteristics for three test devices were obtained as shown in Figs. 9 and 10,

respectively. As shown in Fig. 9, our new model can predict C - V characteristics of the device with high accuracy. Furthermore we have confirmed that the simulated Q factors matched very well with those measured overall gate bias.

IV. CONCLUSIONS

A new RF MOS varactor model has been proposed in this paper. This model consisted of the lumped elements with the physical meanings can be easily implemented in commercial circuit simulators and was successfully validated over frequency up to 18 GHz with S -parameter measurements. Also highly accurate prediction of the C - V and Q - V behaviors with various gate biases was achieved.

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